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Geometry Variations Analysis of TiO_2 Thin-Film and Spintronic Memristors

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***Abstract*–The fourth passive circuit element, memristor, has attracted increased attentions since the first real device was discovered by HP Lab in 2008. Its distinctive characteristic to record the historic profile of the voltage/current through itself creates great potentials in future system design. However, as a nano-scale device, memristor is facing great challenge on process variation control in the manufacturing. In this work, we analyze the impact of the geometry variations on the electrical properties of both TiO_2 thin-film and spintronic memristors, including line edge roughness and thickness fluctuation. A simple algorithm was proposed to generate a large volume of geometry variation-aware three-dimensional device structures for Monte-Carlo simulations. Our simulation results show that due to the different physical mechanisms, TiO_2 thin-film memristor and spintronic memristor demonstrate very different electrical characteristics even when exposing them to the same excitations and under the same process variation conditions.**

I. Introduction

Nearly forty years ago, Professor Chua predicted the existence of memristor – the fourth fundamental circuit element, to complete the set of passive devices that previously includes only resistor, capacitor, and inductor [1]. In 2008, the first physical realization of memristor was demonstrated by HP Lab, in which the memristive effect was achieved by moving the doping front along TiO_2 thin-film device [2]. Soon, memristive systems on spintronic devices were proposed [3].

The unique properties of memristor create great opportunities in future system design. For instance, the non-volatility and excellent scalability make it a promising candidate as the next-generation high-performance high-density storage technology [4]. The applications of memristive behavior [5] in electronic neural network also have been extensively studied [6][7].

As process technology shrinks down to decananometer (sub-50nm) scale, device parameter fluctuations incurred by process variations have become a critical issue affecting the electrical characteristics of devices [8]. The situation in a memristive system could be even worse when utilizing the analog states of the memristor in design. Previous works on memristor variation analysis mainly focused on its impacts on non-volatile memory design [4][9]. However, *the systematic analysis and quantitative evaluation on how process variations affect the memristive behaviors* are still missing. Our work explores the implications of the device parameters of memristors to the circuit design by taking into account the impacts of process variations. The evaluations were conducted based on both theoretical analysis and Monte Carlo simulations.

The device geometry variations significantly influence the electrical properties of nano-devices [10]. For example, the random uncertainties in lithography and patterning processes lead to the random deviations of line edge print-images from its ideal pattern, which is called line edge roughness (LER) [11]. Thickness fluctuation is caused by deposition process in which mounds of atoms form and coarsen over time. As technology shrinks, the geometry variations do not decrease accordingly. In this work, we propose an algorithm to generate a large volume of three-dimensional (3D) memristor structures to mimic the geometry variations. The LER model is based on the latest LER characterization method for electron beam lithography (EBL) technology from top-down scanning electron microscope (SEM) measurement [12]. Other process variations such as random discrete doping (RDD) could also result in the fluctuations of the electrical properties of devices. However, because the existing memristors are all based on the thin film deposition technology, the local randomness of RDD is not as significant as geometry variations, and hence, is not covered in this work.

Memristive function can be achieved by various materials and device structures. The impact of the process variations on the electrical properties of different memristors could be very different even under the same excitations. Two types of devices, TiO_2 thin-film memristor [3] and spintronic memristor [13], are analyzed and evaluated in this work, respectively.

The organization of this paper is as follows: Section II introduces the fundamentals of memristor theory and the physical mechanisms of TiO_2 thin-film memristor and spintronic memristor; Section III analyzes the memristor models under process variations; Section IV explains our proposed algorithm for 3D memristor structure generation;

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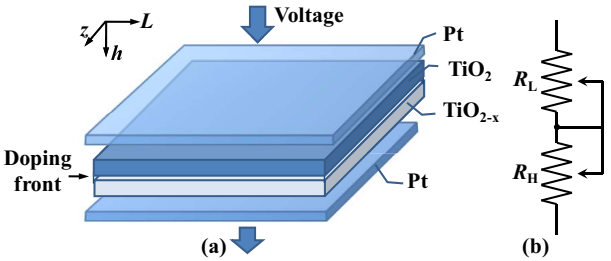

Figure 1. TiO_2 thin-film memristor. (a) structure, and (b) equivalent circuit.

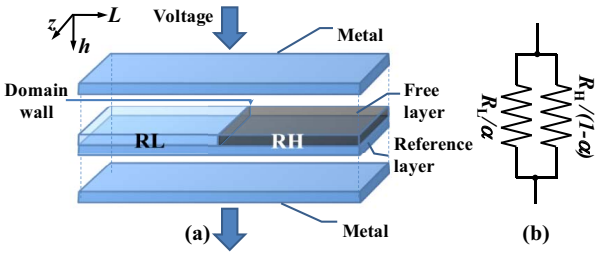

Figure 2. TMR-based spintronic memristor. (a) structure, and (b) equivalent circuit.

Section V presents and analyzes the simulation results of two types of memristors; and Section VI concludes our work.

II. Preliminaries

A. Memristor Theory

The original definition of memristor is derived from the completeness of circuit theory: besides resistor, capacitor and inductor, there must exist the fourth basic two-terminal element that uniquely defines the relationship between the magnetic flux (φ) and the electric charge (q) passing through the device [1], or

$$d\varphi = M \cdot dq. \tag{1}$$

Considering that magnetic flux and electric charge are the integrals of voltage and current over time, respectively, the definition of memristor can be generalized as:

$$\begin{cases} V = M(\omega, I) \cdot I \\ d\omega/dt = f(\omega, I) \end{cases}. \tag{2}$$

Here, ω is a state variable; $M(\omega, I)$ represents the instantaneous memristance, which varies over time. For a "pure" memristor, neither $M(\omega, I)$ nor $f(\omega, I)$ is an explicit function of I [5].

B. TiO_2 Thin-film Memristor

In 2008, HP Lab demonstrated the first memristive device in TiO_2 thin-film [2]. Figure 1 illustrates the conceptual view and the corresponding variable resistor model, which is equivalent to two series-connected resistors. Here, R_L (R_H) is used to denote the lowest (highest) resistance. The overall resistance can be expressed as

$$M(\alpha) = \alpha \cdot R_L + (1 - \alpha) \cdot R_H. \tag{3}$$

$\alpha\ (0 \le \alpha \le 1)$ is the relative doping front position, which is the ratio of doping front position over the total thickness of TiO_2 thin-film. The velocity of doping front movement *v(t)*, which is driven by the voltage applied across the memristor V(t) can be expressed as

$$v(t) = \frac{d\alpha(t)}{dt} = \mu_v \cdot \frac{R_L}{h^2} \cdot \frac{V(t)}{M(\alpha)}, \tag{4}$$

where, μ_v is the equivalent mobility of dopants; h is the total thickness of the TiO_2 thin film; and *M(a)* is the total memristance when the relative doping front position is α.

C. Spintronic Memristor

Among all the spintronic memristive devices proposed recently, the one based on magnetic tunneling junction (MTJ) could be the most promising one because of its simple structure [3][13]. We choose tunneling magneto-resistance (TMR)-based structure illustrated in Figure 2(a) as the objective of this work. The lowest (highest) resistance is denoted as R_L (R_H).

As shown in Figure 2(b), the overall resistance of a TMR-base spintronic memristor can be modeled as two parallel-connected resistors with resistances R_L/α and $R_H/(1-\alpha)$, respectively [13]. Here α $(0 \le \alpha \le 1)$ represents the relative domain wall position as the ratio of the domain wall position (x) over the total length of the free layer (L). The overall memristance can be expressed as

$$M(\alpha) = \frac{R_H \cdot R_L}{R_H \cdot \alpha + R_L \cdot (1-\alpha)}. \tag{5}$$

The domain-wall velocity *v(t)* is proportional to the current density J [14]. We have

$$J(t) = \frac{V(t)}{M(\alpha) \cdot L \cdot z}, \text{ and} \tag{6}$$

$$v(t) = \frac{d\alpha(t)}{dt} = \frac{\Gamma_v}{L} \cdot J_{eff}(t), \quad J_{eff} = \begin{cases} J, & J \ge J_{cr} \\ 0, & J < J_{cr} \end{cases}. \tag{7}$$

Here Γ_v is the domain wall velocity coefficient, which is related to device structure and material property. L and z are the total length and width of the spintronic memristor, respectively. The domain wall movement in a spintronic memristor happens only when the current density $J(t)$ is above the critical current density (J_{cr}) [14] [15].

III. Statistical Analysis

The actual length (L) and width (z) of a memristor is affected by line edge roughness (LER). The variation of thickness (h) of a thin film structure is usually described by thickness fluctuations. As a matter of convenience, we define that, the impact of process variations on any given variable can be expressed as a factor $\theta = \omega'/\omega$, where ω is the ideal value, and ω' is the actual value under process variations. The ideal geometry dimensions of TiO_2 thin-film memristor and spintronic memristor used in this work are summarized in TABLE I [2][13].

A. TiO2 Thin-Film Memristor

In a TiO_2 thin-film memristor, the current passes through

TABLE I. THE DEVICE DIMENSIONS OF MEMRISTORS.

	Length (L)	Width (z)	Thickness (h)
Thin-film	50 nm	50 nm	10 nm
Spintronic	200 nm	10 nm	7 nm

the device along thickness (h) direction. Ideally the doping front has an area $S=L\cdot z$. To simulate the impact of LER on the electrical properties, the memristor device is divided into many small filaments between the two electrodes. Each filament i has a cross-section area ds and a thickness h. The ideal upper bound and lower bound of the memristance for filament i are

$$R_{i,H} = R_H \cdot \frac{S}{ds}, \text{ and } R_{i,L} = R_L \cdot \frac{S}{ds}. \quad (8)$$

For filament i, the actual upper and the lower bound under the process variations can be expressed as

$$R'_{i,H} = R_{i,H} \cdot \frac{\theta_{i,h}}{\theta_{i,s}}, \text{ and } R'_{i,L} = R_{i,L} \cdot \frac{\theta_{i,h}}{\theta_{i,s}}. \quad (9)$$

Here $\theta_{i,s}$ and $\theta_{i,h}$ represent the variations caused by 2-D LER and thickness fluctuations, respectively.

The doping front velocity in filament i by considering process variations can be calculated as:

$$v'_i(t) = \mu_v \cdot \frac{R'_{i,L}}{h'^2} \cdot \frac{V(t)}{M'_i(\alpha'_i)}. \quad (10)$$

Here h' and M'_i are the actual thickness and memristance of filament i. Then, we can get a set of related equations for filament i, including the doping front position

$$\alpha'_i(t) = \int_0^t v'_i(\tau) \cdot d\tau, \quad (11)$$

the corresponding memristance

$$M'_i(\alpha'_i) = \alpha'_i \cdot R'_{i,L} + (1-\alpha'_i) \cdot R'_{i,H}, \quad (12)$$

and the current through the filament i

$$I'_i(t) = \frac{V(t)}{M'_i(\alpha'_i(t))}. \quad (13)$$

By combining Eq. (10) – (13), the doping front position in every filament i under process variations $a'_i(t)$ can be obtained by solving the differential equation

$$\frac{da'_i(t)}{dt} = \mu_v \cdot \frac{R'_{i,L}}{h'^2} \cdot \frac{V(t)}{a'_i(t)\cdot R'_{i,L} + (1-a'_i(t))\cdot R'_{i,H}}. \quad (14)$$

Eq. (14) indicates that the behavior of the doping front movement is dependent on the specific electrical excitations, i.e., $V(t)$. For instance, if applying a sinusoidal voltage source such as

$$V = V_m \cdot \sin(2\pi f \cdot t), \quad (15)$$

the corresponding doping front position of filament i can be expressed as:

$$a'_i(t) = \frac{R_{i,H} - \sqrt{R_{i,H}^2 + A\cdot B(t)\cdot\frac{1}{\theta_{i,h}^2} - 2C[1]\cdot A\cdot\frac{\theta_{i,s}}{\theta_{i,h}}}}{A}, \quad 0 \le a'_i \le 1. \quad (16)$$

Where, $A = R_{i,H} - R_{i,L}$, $B(t) = \mu_v \cdot R_{i,L} \cdot V_m \cdot \frac{\cos(2\pi f\cdot t)}{f\cdot h^2\cdot\pi}$, and C[1] is an initial state constant.

The existence of term $B(t)$ stands for the impact of electrical excitation on doping front position. The terms $\theta_{i,s}$ and $\theta_{i,h}$ stand for the impact of both LER and thickness fluctuations on memristive behavior, respectively. Moreover, the impact of the geometry variations on the electrical properties of memristors could be affected by the electrical excitations. For example, we can set $a(0) = 0$ to represent the case that the TiO_2 memristor starts from $M(0)=R_H$. In such a condition, the doping front position $a'_i(t)$ can be calculated as:

$$a'_i(t) = \frac{R_{i,H} - \sqrt{R_{i,H}^2 + A\cdot B(t)\cdot\frac{1}{\theta_{i,h}^2} - A\cdot B(0)\cdot\frac{1}{\theta_{i,h}^2}}}{A}, \quad 0 \le a'_i \le 1, \quad (17)$$

which is affected only by thickness fluctuations and electrical excitations. LER won't disturb $a'_i(t)$ if the TiO_2 thin-film memristor has an initial state $a(0) = 0$.

The overall memristance of the memristor can be calculated as the total resistance of all n filaments connected in parallel. When n increases to ∞, we have

$$R'_H = R_H \cdot \frac{1}{\int_0^\infty \theta_{i,h}/\theta_{i,s}\cdot di}, \text{ and } R'_L = R_L \cdot \frac{1}{\int_0^\infty \theta_{i,h}/\theta_{i,s}\cdot di}. \quad (18)$$

The overall current through the memristor is the sum of the current through each filament:

$$I'(t) = \int_0^\infty I'_i(t) \cdot di. \quad (19)$$

The instantaneous memristance of the overall memristor can be defined as

$$M'(t) = \frac{V(t)}{I'(t)} = \frac{1}{\int_0^\infty 1/M'_i\cdot di}. \quad (20)$$

Considering that the doping front movement in each filament won't be the same because h'_i varies due to thickness fluctuation (and/or the roughness of the electrode contact), we define the average doping front position of the whole memristor as:

$$\alpha'(t) = \frac{R'_H - M'(t)}{R'_H - R'_L}. \quad (21)$$

B. Spintronic Memristor

Because the length of a spintronic memristor is usually much longer than the other dimensions, the impact of the variance in length on the device's electrical properties can be ignored. In our analysis, the device can be chopped into infinite segments in the length direction. For a segment i, the upper and lower bounds of memristance are

$$R'_{i,H} = R_{i,H} \cdot \frac{\theta_{i,h}}{\theta_{i,z}}, \text{ and } R'_{i,L} = R_{i,L} \cdot \frac{\theta_{i,h}}{\theta_{i,z}}. \quad (22)$$

Here we assume the ideal memristance changes linearly within the domain wall, or $R_{i,H}$ changes linearly from $R_{j,L}$ to $R_{k,H}$ when $j < i < k$. Here j and k are the two segments at the two boundaries of domain wall and connected to the magnetic domains with either the low or the high resistance states. The memristance of each segment is

$$M'_i(\alpha') = \begin{cases} R'_{i,L}, & i < \alpha' \\ R'_{i,H}, & i \ge \alpha' \end{cases}. \quad (23)$$

So for overall resistance R'_H and R'_L, we have

$$R'_H \cdot \frac{1}{\int_0^\infty \theta_{i,z}/\theta_{i,h}\cdot di}, \text{ and } R'_L = R_L \cdot \frac{1}{\int_0^\infty \theta_{i,z}/\theta_{i,h}\cdot di}. \quad (24)$$

Then the memristance of the whole device is

$$M'(a') = \frac{1}{\int_0^{a'} \frac{1}{R'_{i,L}} d(i) + \int_{a'}^1 \frac{1}{R'_{i,H}} d(i)} = \frac{1}{\int_0^{a'} \frac{1}{R_{i,L}}\frac{\theta_{i,z}}{\theta_{i,h}} d(i) + \int_{a'}^1 \frac{1}{R_{i,H}}\frac{\theta_{i,z}}{\theta_{i,h}} d(i)}. \quad (25)$$

Here the width of every segments z_i varies segment by segment due to the LER effect. The statistical behavior of

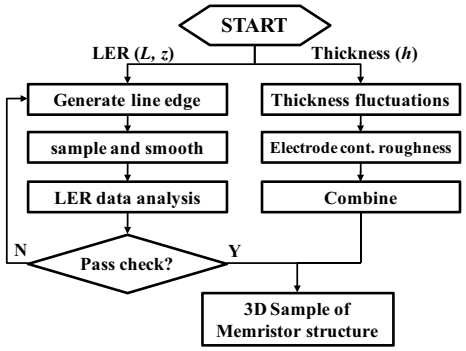

Figure 3. The flow of 3D memristor structure generation including geometry variations.

spintronic memristors can still be evaluated by Monte-Carlo simulation in Section V.

We assume the current density applied on the domain wall $J'(t)$ is the one of the segments i in which the middle of domain wall located:

$$J'(t) = J'_i = \frac{V(t)}{M'(a')\cdot L\cdot z'_i}, \quad (26)$$

Then the domain wall velocity under process variations can be calculated as:

$$v'(t) = v'_i = \frac{d\alpha'(t)}{dt} = \frac{\Gamma_v}{L}\cdot J'_{eff}(t), \quad J_{eff} = \begin{cases} J', & J' \geq J_{cr} \\ 0, & J' < J_{cr} \end{cases}. \quad (27)$$

IV. 3D Memristor Structure Modeling

Analytic modeling is a fast way to estimate the impacts of process variations on memristors. However, we noticed that modeling some variations analytically e.g. LER may be beyond the capability of analytic model [12]. The silicon data of these variations, however, is usually very hard to obtain simply due to intelligent property protection. To improve the accuracy of our evaluations, we create a simulation flow to generate 3D memristor samples with the geometry variations including LER and thickness fluctuation. The correlation between the generated samples and the real silicon data are guaranteed by the sanity check of the LER characterization parameters. The flow is shown in Figure 3.

Many factors affecting the quality of the line edges show different random effects. Usually statistical parameters such as auto-correlation function (ACF) and power spectral density (PSD) are used to describe the property of the line edges. Considering that LER issue is related to fabrication process, we mainly target the nano-scale pattern fabricated by electron beam lithography (EBL). The measurements show that under such a condition, the line edge profile has two important properties: (1) the line edge profile demonstrates regular oscillations, which are caused by periodic composition in EBL fabrication system; and (2) the line edge roughness mainly concentrates in a low frequency zone [12].

TABLE II. THE PARAMETERS/CONSTRAINTS IN LER CHARACTERIZATION.

Parameters		Constraints	
L_{LF}	0.8 nm	σ_{LER}	2.5nm ~ 3.5nm
f_{max}	1.8 MHz	σ_{LWR}	4.0nm ~ 5.0 nm
L_{HF}	0.4 nm	*skewness*	0.1 ~ 0.2
/	/	*kurtosis*	2.9 ~ 3.1

TABLE III. MEMRISTOR DEVICE AND ELECTRICAL PARAMETERS.

TiO2 thin-film memristor [2]					
R_L (Ω)	R_H (Ω)	μ_v ($m^2 \cdot s^{-1} \cdot V^{-1}$)	/	V_m (V)	f (Hz)
100	16000	10^{-14}	/	1	0.5
Spintronic memristor [13]					
R_L (Ω)	R_H (Ω)	Γ_v ($nm^3 \cdot C^{-1}$)	J_{cr} (A/nm^2)	V_m (V)	f (Hz)
2500	7500	2.01×10^{16}	2.00×10^{-8}	2	10M

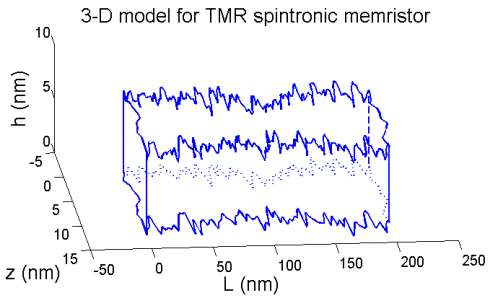

Figure 4. An example of 3-D memristor structure.

To generate line edge samples close to the real cases, we can equally divide the whole line edge into many segments, say, n segments. The LER of the i^{th} segment can be modeled by

$$LER_i = L_{LF}\cdot \sin(f_{max}\cdot x_i) + L_{HF}\cdot p_i. \quad (28)$$

The first term in the right side of Eq. (28) represents the regular disturbance at the low frequency range, which is modeled as a sinusoid function with amplitude L_{LF}. f_{max} is the mean of the low frequency range derived from PSD analysis. Without loss of generality, an uniform distribution $x_i \in U(-1,1)$ is used to represent an equal distribution of all frequency components in the low frequency range. The disturbance from high frequency domain is also taken into account by the second term on the right side of Eq. (28) as a Gaussian white noise with amplitude L_{HF}. Here p_i follows the normal distribution $\mathcal{N}(0,1)$ [12]. The actual values of L_{LF}, L_{HF} and f_{max} are determined by ACF and PSD.

To ensure the correlation between the generated line edge samples with the measurement results, we introduce four constraints to conduct sanity check of the generated samples:

- σ_{LER}: the root mean square (RMS) of LER;
- σ_{LWR}: the RMS of line width roughness (LWR);
- skewness: the symmetry of the amplitude of the line edge; and
- kurtosis: the steepness of the amplitude distribution curve.

The above four parameters are widely received in LER characterization and can be achieved from measurement results directly. Only the line edge samples that satisfy the constraints will be taken for the Monte-Carlo simulations. TABLE II summarizes the parameters used in our algorithm, which are correlated with the characterization method and experimental results in [12].

The thickness fluctuation is caused by the random uncertainties in sputter deposition or atomic layer deposition.

TABLE IV. 3σ MIN./MAX. OF TIO2 MEMRISTOR PARAMETERS.

Sinusoidal Voltage	LER only		Thickness only		Overall	
	–3σ	+3σ	–3σ	+3σ	–3σ	+3σ
R_H & R_L	-5.4%	4.1%	-5.5%	4.8%	-6.4%	7.3%
$M(\alpha)$	-5.4%	4.1%	-37.1%	20.8%	-36.5%	24.1%
$\alpha(t)$	0.0%	0.0%	-13.3%	27.5%	-14.7%	27.4%
$v(\alpha)$	0.0%	0.0%	-9.3%	15.6%	-10.4%	16.9%
$i(\alpha)$	-4.7%	5.7%	-9.3%	15.7%	-10.7%	17.2%
Power	-4.7%	5.7%	-8.8%	14.1%	-10.1%	15.6%

It has a relatively smaller impact than LER and can be modeled as Gaussian distribution. Considering that the memristors in this work have relatively bigger dimensions in horizontal plane than thickness direction (shown in TABLE I), we also considered roughness of electrode contact in our simulation: The means of the thickness of every memristors are generated by assuming it follows the Gaussian distribution among all simulated memristors. Then every memristor is divided into many filaments between the two electrodes. The roughness of electrode contracts is modeled as the disturbance on the thickness of each filament. We assume that both thickness fluctuations and electrode contact roughness follow Gaussian distributions with a deviation σ=2% of thin film thickness.

Figure 4 is an example of 3-D spintronic memristor structure generated by our flow.

V. Experimental Results

A. Simulation Setup

To evaluate the impacts of process variations on the electrical properties of memristors, we conducted Monte-Carlo simulations with 10,000 qualified 3-D device samples generated by our proposed flow. A sinusoidal voltage source in Eq. (15) is applied as excitation. The initial state of memristor is set as $M(\alpha=0)=R_H$. The device and electrical parameters used in our simulations are summarized in TABLE III. Both separated and combined effects of geometry variations on various electrical properties are analyzed, including:

- the distribution of R_H and R_L;
- the change of memristance $M(t)$ and $M(\alpha)$;
- the velocity of wall movement $v(\alpha)$;
- the current through memristor $i(t)$; and
- the I-V characteristics.

B. TiO_2 Thin-Film Memristor

For TiO_2 thin-film memristors, the ±3σ (minimal/ maximal) values of the device/electrical parameters in the percentage of the corresponding ideal values are summarized in TABLE IV. For those parameters that vary over time, we consider the variation at each time step of all the devices. The simulation results considering only either LER or thickness fluctuations are also listed. To visually demonstrate the overall impact of process variations on the memristive behavior, the dynamic responses of 100 Monte Carlo simulations are shown in Figure 5.

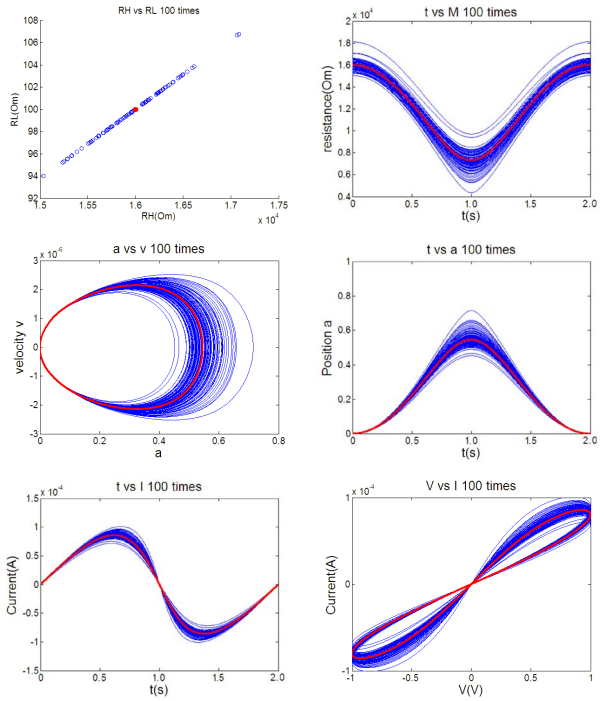

Figure 5. Simulation results for TiO_2 thin-film memristors. The blue curves are from 100 Monte-Carlo simulations, and red lines are the ideal condition. From top left to right bottom, the figures are R_H vs. R_L; $M(t)$ vs. t; v vs. α; α vs. t; I vs. t; and I-V characteristics.

TABLE IV shows that the static behavior parameters, i.e., R_H and R_L, are affected in a similar range by LER and thickness fluctuations. This is consistent to the analytical results in Eq. (18): θ_s and θ_h have the similar weights on the variation of R'_H and R'_L.

However, thickness fluctuations show a much more significant impact on the memristive behaviors such as $v(t)$, $\alpha(t)$ and $M(\alpha)$, than LER does because the doping front movement is along the thickness direction: $v(t)$ is inversely proportional to the square of thickness, and $\alpha(t)$ is the integral of $v(t)$ over time as shown in Eq. (10) and (11). Due to the similar reason, thickness fluctuations significantly affect the instantaneous memristance $M(\alpha)$ as well.

Since the thickness of TiO_2 thin-film memristor is relatively small compared to other dimensions, we assume the doping front cross-section area is a constant along thickness direction in our simulation. The impacts of LER on $\alpha(t)$ or $v(t)$ are negligible compared to that of the thickness fluctuation as shown in TABLE IV.

An interesting observation in Figure 5 is that as the doping front α moves toward 1, the velocity v regularly grows larger and reaches its peak at the half period of the sinusoidal excitation, i.e. t=1s. This can be explained by Eq. (16): the memristance is getting smaller as α moves toward 1. With the same input amplitude, a smaller resistance will result in a bigger current and therefore a bigger variation on $v(t)$. Similarly, memristance $M(\alpha)$ reaches its peak variance when α is close to 1.

C. Spintronic Memristor

TABLE V. 3σ MIN./MAX. OF SPINTRONIC MEMRISTOR PARAMETERS.

Sinusoidal Voltage	LER only		Thickness only		Overall	
	−3σ	+3σ	−3σ	+3σ	−3σ	+3σ
R_H & R_L	-15.3%	22.9%	-6.1%	5.8%	-16.4%	20.9%
$M(\alpha)$	-15.1%	23.3%	-11.0%	11.0%	-16.3%	21.1%
$\alpha(t)$	-9.7%	8.1%	-8.4%	9.5%	-11.8%	8.1%
$v(\alpha)$	-10.7%	22.1%	-9.1%	9.9%	-21.5%	22.5%
$i(\alpha)$	-18.5%	18.5%	-8.9%	10.1%	-17.7%	17.8%
Power	-18.4%	18.6%	-8.3%	9.4%	-17.8%	17.8%

The ±3σ values of the device/electrical parameters based on 10,000 Monte-Carlo simulations for spintronic memristors are summarized in TABLE V. The visual demonstration of 100 Monte-Carlo simulations with a sinusoidal voltage excitation is shown in Figure 6.

In spintronic memristors, the impact of LER is more than that of thickness fluctuations. This is because the direction of the domain wall movement is perpendicular to the direction of spin-polarized current. The impacts of thickness fluctuations on very small segments cancel each other during the integral along the direction of the domain wall movement.

"LER only" simulation results show more impact on the electrical properties at +3σ corner than that at −3σ corner. This is because the variation of line width is the dominant factor of the variation of electrical properties of spintronic memristors and the line edge profiles used in our LER parameters have a right-biased feature [12]. Since normal distribution is assumed for the variations of thickness, θ_h has approximately symmetric impacts on ±3σ corners

The impact of LER on the memristive parameters $v(t)$, $\alpha(t)$ and $M(\alpha)$ is also larger than thickness variations. Again, the impacts of thickness fluctuations on very small segments cancel each other during the integral along the direction of the domain wall movement.

VI.Conclusion

In this work, we evaluate the impact of different geometry variations on the electrical properties of two different types of memristors – TiO_2 thin-film and spintronic memristors, by conducting the analytic modeling analysis and Monte-Carlo simulations. We investigate the different responses of the static and memristive parameters under various process variations and explore its implication to the electrical properties of the memristors. A simple LER sample generation algorithm is proposed to speed up the related Monte-Carlo simulations. To author's best knowledge, this is the first work that conduct the quantitative evaluation and comparison on the impact of geometry variations to the two types of memristors.

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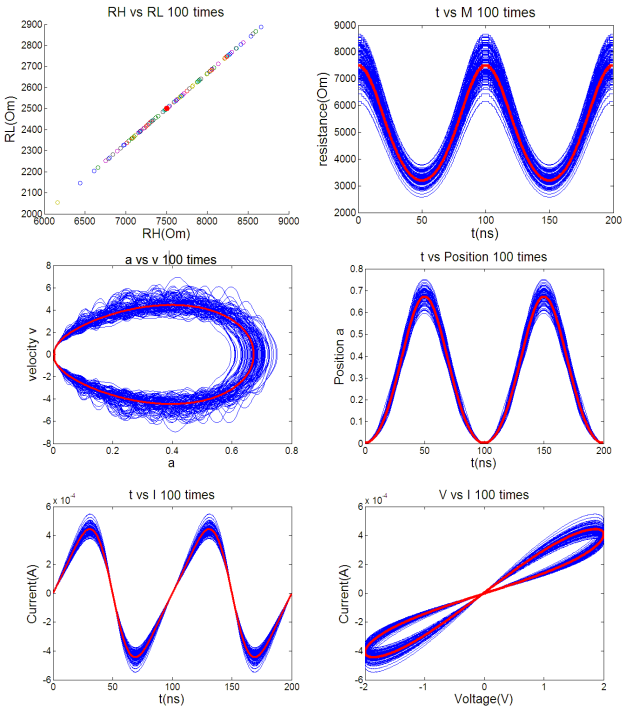

Figure 6. Simulation results for spintronic memristors. The blue curves are from 100 Monte-Carlo simulations, and red lines are the ideal condition. From top left to right bottom, the figures are R_H vs. R_L; $M(t)$ vs. t; v vs. α; α vs. t; I vs. t; and I-V characteristics.

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